ABSTRACT OF THE DISCLOSURE

To reduce electric current concentration and electric field concentration in junction parts even in the case of miniaturization, and to achieve triggering at low voltage, an ESD protection apparatus is installed between an input terminal of a semiconductor integrated circuit chip and a CMOS transistor. The ESD protection apparatus includes a trigger element having diodes which are broken down by overvoltage applied to the input terminal and an ESD protection element including vertical bipolar transistors for discharging the accumulated electric charge of the input terminal by being electrically discharged owing to the breakdown of the diodes.